#11/Appeal Brief 21363

Attorney's Docket No. 042390.P6126D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application for:

Makarem A. Hussein

Serial No.: 09/672,375

Filed: September 28, 2000

For: **A PROCESS TO MANUFACTURE CONTINUOUS METAL INTERCONNECTS**

Examiner: Owens, Douglas W.

Art Unit: 2811

APPEAL BRIEF

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Applicant submit, in triplicate, the following Appeal Brief pursuant to 37 C.F.R. § 1.192 for consideration by the Board of Patent Appeals and Interferences. Applicant also submits herewith a check in the amount of $320.00 to cover the cost of filing the opening brief as required by 37 C.F.R. §1.17(c). Please change any additional amount due or credit any overpayment to the Deposit Account 02-2666.

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I. REAL PARTY IN INTEREST

The real party in interest is Intel Corporation, of Santa Clara, California.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences which will affect or be affected by the outcome of this appeal.

III. STATUS OF THE CLAIMS

Claims 12-17 are pending and rejected in this application. Claims 1-11 have been canceled and form no part of this appeal.

IV. STATUS OF THE AMENDMENTS

No amendment has been filed subsequent to the final rejection.

V. SUMMARY

The pending claims relate to metal interconnects for integrated circuits. For example, an integrated circuit may include a substrate having a circuit device and a dielectric material overlying the circuit device with a via formed in the dielectric material to the circuit device and exposing a sidewall in the dielectric material and a surface of the circuit device. (Applicant's specification, page 7, line 22 through page 8, line 21) Substantially lining the sidewall of the dielectric material is barrier material and a seed layer is on the barrier material, also substantially lining the sidewall. (Applicant's specification, page 9, lines 5-24) In addition, a conductive material directly contacts the surface of the circuit device. (Applicant's specification, page 11, line 19 through page 12, line 9) Moreover, the barrier material can be chosen to have sufficiently different etch characteristics than the seed material that is subsequently applied. (Page 9, lines 13-15) Specifically, for example, a copper seed material may be deposited using a standard sputter deposition technique to define a thickness of 100% on the top of the dielectric the via is formed in, 40% along the sidewalls of the via, and 5% at the bottom of the via (substantially exposing the barrier layer there due to the insignificant amount of seed material deposited on the bottom surface). (Page 10, lines 10-24, Figures 3 and 4)

Particularly, the material chosen for the barrier material can have sufficiently different etch characteristics than the seed material such that the seed material may act as a mask to protect the barrier material along the via walls, and trench, during etching of the barrier material at the via bottom so that continuous interconnect lines may be formed on the substrate and connect directly to the circuit device below without intervening barrier material between the interconnect and the circuit device below. (Page 11, line 4 through page 12, line 9, Figures 5 and 6)

VI. ISSUES

The issues involved in this appeal are as follows:

A. Are claims 12-17 unpatentable under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,323,131 B1 issued to Obeng, et al. ("Obeng")?

VII. GROUPING OF THE CLAIMS

Applicant submits that the claims do not stand or fall together. Applicant groups the claims on appeal as follows:

Group I : Claims 12-14
Group II : Claim 15
Group III : Claim 16
Group IV : Claim 17

Applicant will argue why each of these groups of claims should be allowed below.

VIII. ARGUMENT

The Examiner has rejected claims 12-17 under 35 U.S.C. §102(e) as being anticipated by Obeng.

A. Overview of the Cited References

Obeng

Obeng teaches copper interconnects with a self assembling organic film and a seed layer deposited in the trench and via under the copper interconnect to provide a barrier layer against copper migration, as well as a corrosive protection passivating

layer of self assembling organic film formed on the top surface of the interconnect by treating the copper surface with a dilute solution. (Abstract, and col. 4, lines 8-35) Obeng describes the use of the self assembled films integrated into existing processing steps, such as by depositing a thin diffusion barrier/adhesion promoter film 18 of self assembling organic film along a trench and via etched in a silicon substrate, followed by the deposition of a copper seed layer which is then capped with a thick copper film 20 by known techniques. (Col. 4, lines 9-25) The thick copper film 20 is then polished and the remaining exposed copper layer 22 is then covered with spontaneous self assembling film 24. (Col. 4, lines 25-33) Thus, a layer of interconnect is formed having thin diffusion barrier/adhesion promoter film 18 and a seed layer between thick copper film 20 and the structure below the copper film, as well as having a spontaneous self assembling film 24 over any exposed top of the copper layer 22, as shown in Figure 1(*c*). (Col. 4, lines 20-33, Figures 1(*a*) - 1(*c*)) Subsequently, the above steps may then be repeated as required to form a device having multilayer interconnections. (Col. 4, lines 33-34)

B. Errors of Law and Fact

1) Specific limitations of Group I not described in the cited references.

Claims 12-14 require (as claims 13 through 14 depend from claim 12): a conductive material directly contacting a surface of the circuit device.

2) Explanation as to why such limitations render Group I unanticipated by the cited references.

Claims 12-14 are not anticipated by Obeng for at least the reason that Obeng does not describe a conductive material directly contacting the surface of the circuit device, as required by independent claim 12. It is axiomatic that to be anticipated every element of a claim must be disclosed within a single reference. In the Patent Office's rejection of claim 12, the Patent Office cites conductive material 20 and Figure 1(*d*) of Obeng against the above cited limitation of independent claim 12.

Obeng describes forming copper interconnects in circuits by lining circuit trenches and vias with a self-assembling organic film barrier layer, depositing a seed layer over the barrier layer, and then capping the seed layer with a thick copper film. For instance, at col. 4, lines 21-24, Obeng states:

> A thin diffusion barrier/adhesion promoter film 18 may the be deposited, which again may be a self assembling organic film, followed by the deposition of a copper seed layer which is then capped with a thick copper film 20 by known techniques to give rise to the structure shown in FIG. 1(b). [Emphasis added]

Obeng then describes polishing the thick copper layer down to the dielectric layer, and then passivating the exposed copper and dielectric layer with a layer of spontaneous self-assembling film 24. Obeng goes on to say that the above steps can be repeated to form a device having multi-level interconnects. For example, at col. 4, lines 33-35 Obeng states:

> The above steps may then be repeated as required to form a device having multilevel interconnections as shown in **FIG. 1(*d*)**. [Emphasis added]

However, the Patent Office has not identified and the Applicant has been unable to find any description in Obeng of removing either barrier film 18 or the copper seed layer deposited in the via, or of removing spontaneous self-assembling film 24. Thus, since Obeng fails to mention removing any portion of diffusion barrier/adhesion promoter film 18, copper seed layer, or spontaneous self-assembling film 24, a second level of interconnects formed over the structure shown in Figure 1(*c*) would include at least those three layers between the second level of interconnects and the first layer. Therefore, in any instance of capping a via with thick copper film 20, Obeng teaches thick copper film 20 capped over at least diffusion film 18 and a copper seed layer. It is unfortunate that the figures in Obeng (*e.g.*, Figure 1(*d*)) are vague and appear to indicate a structure other than that described by the text of Obeng. The teachings of Obeng are not consistent with the figures in this instance.

In contrast to Obeng, Applicant's claim 12 includes "a conductive material directly contacting the surface of the circuit device." [Emphasis added] Therefore, the direct contact required in claim 12 is not described by the barrier film 18 and copper seed layer between thick copper film 20 and a circuit device below "by known techniques" no matter how many levels are formed in Obeng. In other words, the "remaining exposed copper layer 22" cited by the Patent Office is exposed only between the time it is polished in the CMP processing and the time passivating spontaneous self-assembling film 24, as shown in Figure 1(*c*) is deposited over it.

In the Advisory Action mailed November 13, 2002, the Patent Office is unconvinced by the Applicant's arguments filed October 23, 2002 that Figure 1(*d*) of Obeng is not consistent with Obeng's teachings and that the mention of "the remaining exposed copper layer 22" at col. 4, line 31 of Obeng, does not result in a direct connection between copper layer 22 and subsequent interconnect 20, as shown in Figure 1(*d*). Applicant respectfully disagrees and addresses the Patent Office's comments. Applicant asserts that the omissions of layer 18 at the bottom of the via in Figure 1(*c*), and the omission of layer 24, layer 18, and a seed layer between second copper layer 20 and interconnect structure below of Figure 1(*d*) are inconsistencies in the figures and in error with respect to the detailed description. First, Figure 1(*d*) is inaccurate because, as noted above, the Detailed Description of Obeng only describes thick copper film 20 capping the seed layer and the barrier film. For example, at col. 4, lines 21-24 Obeng describes diffusion barrier 18 and a copper seed layer in the via between thick copper film 20 and underlying silicon substrate 12. Thus, the formation of the subsequent or second level conductive material 20 on the left side of Figure 1(*d*), requires that subsequent or second level of the interconnect structure be formed by repeating the steps previously described (and the only steps described in Obeng for depositing thick copper film 20 with respect to Figure 1) of leaving film 18 and a copper seed layer between the conductive material 20 and the structure below it. Obeng requires that all subsequent layers of interconnections be formed repeating the above steps as required. (Obeng, col. 4, lines 33-36) Specifically, the structures in Figure 1(*d*) formed over the structures of Figure 1(*c*) are formed by repeating the steps described at col. 4, lines 21-24 of Obeng and shown in Figures 1(*a*)-1(*b*). Film 24, barrier/adhesion promoter film 18, and a seed layer would exist above the previously exposed first copper layer because once the second layer of dielectric layer 10 deposited in Figure 1(*d*) above the first circuit level (*e.g.*, the level shown in Figure 1(*c*)) was etched to form the second layer trench and via, it would be necessary to again deposit diffusion barrier/adhesion promoter film 18 and a seed layer in the second layer trench and via before depositing the second layer thick copper film 20 interconnect. Thus it is clear that the film 18 and copper seed layer shown in Figure 1(*b*) must also exist between conductive material 20 and the interconnect structure circuit device that is formed in the insulative portion of the substrate in Figures 1(*c*) and 1(*d*).

In addition, the showing of diffusion barrier/adhesion promoter film 18 and the dark line seed layer in Figure 1(*b*) under copper 20, is inconsistent with the omission of layer 18 in Figures 1(*c*) and 1(*d*) because there is no description in Obeng of removing layer 18 from the bottom of the via and once copper layer 20 is deposited in the via, layer 18 must remain at the bottom of the via sandwiched between copper layer 20 and the structure 12, below (*e.g.*, see layer 18 along the sidewalls of the via and trench in Figures 1(*c*) and 1(*d*)). Moreover, since there is no description of removing passivating film 24 from the top of structure 1(c), that film, as well as layer 18 and a seed layer, as shown in Figure 1(*b*) would exist between the second level copper interconnect 20 and the structure below shown in Figure 1(*d*). For instance, at col. 4, lines 31-33 of Obeng and as admitted by the Patent Office, in the Advisory Action mailed November 13, 2002, exposed copper layer 22 is passivated with self-assembling film 24, as shown in Figure 1(*c*). However, there is no description in Obeng of removing film 24, as shown in Figure 1(*c*), prior to Figure 1(*d*). Thus, Applicant asserts that Figures 1(*c*) and 1(*d*) are in error, and do not cure the fact that the Detailed Description of Obeng fails to mention any removal of diffusion barrier layer 18, copper seed layer, or passivation layer 24. In other words, the "remaining exposed copper layer 22" cited by the Patent Office is exposed only between the time it is polished in the CMP processing and the time passivating spontaneous self-assembling film 24, as shown in Figure 1(*c*) is deposited over it.

As a result, the statements by the Patent Office in the Advisory Action that "the applicant argues that the barrier/adhesion layer 'showed' exists between the first copper layer (22) and the second layer (20), reasoning that this is so because Obeng et al. would have repeated the same steps used to form the first conductive layers. The Applicant has provided no support for this argument" are untrue. The Applicant indicated in the Response to Final Office Action of October 23, 2002, and clarifies herein, that Obeng must repeat the same steps used to form the first conductive layers. (Obeng, col. 4, lines 33-36)

On the contrary, the Patent Office's statement in the Advisory Action that "Obeng et al. explicitly states that copper layer 22 is exposed in lines 31-33 of col. 4" is true. However, this does not result in copper layer 22 directly contacting the second layer interconnect 20 formed above it. Particularly, as described above, and as stated in

the portion of Obeng cited by the Patent Office "the remaining exposed copper layer 22 is then passivated with a spontaneous self-assembling film 24 as described above." [Emphasis added] Thus, it is clear that copper layer 22 is exposed by the CMP processing, then is covered with film 24, and subsequently processed according to Figures 1(*a*) and 1(*b*), as described above.

Furthermore, Obeng describes depositing barrier, seed and interconnect layers using "known techniques." As practiced in the art, "known techniques" of capping a circuit device with thick copper film 20 include capping a barrier layer and a seed layer between the thick copper film 20 and any structure below and do not include removal of the seed layer. (See Applicant's specification, Background section, page 1, line 14 through page 2, line 6) More particularly, known techniques of forming an interconnect by depositing copper into a trench and via lined with a barrier layer and seed layer certainly do not include lining circuit trenches and vias with a self-assembling organic film barrier layer in the manner which Obeng, bases its inventiveness on. Therefore, as the Patent Office should agree, if the self-assembling organic film barrier layer 18 or 24, as shown in Figures 1(*b*) and 1(*c*) were to be removed, such removal could not be "a known technique" because removal would also be part of the inventive technology on which Obeng is based. Thus, removal of layer 18 or 24 is not described in Obeng and is not a "known technique."

Therefore, a conductive material directly contacting the surface of the circuit device, in accordance with Applicant's independent claim 12, is not described by the forming of interconnects related to Figure 1 of Obeng, which require diffusion barrier/adhesion promoter film 18 and a seed layer between interconnect thick copper film 20 and any structure below film 20, and which require passivating film 24 between subsequent layers.

3) Specific limitations of Group II not described in the cited references.

Throughout the following argument, it is assumed that the dependent claims carry with them the arguments made in favor of base claims and any intervening claims.

Claims 15 further requires that the barrier layer comprises an etch characteristic such that the barrier material can be selectively etched in the presence of the seed material.

4) Explanation as to why such limitations render Group II unanticipated by the cited references.

Applicant submits that dependent claim 15 is further not anticipated by Obeng for at least the reason that Obeng does not describe a barrier layer with etch characteristics so that the barrier material can be selectively etched in the presence of the seed material.

Applicant's dependent claim 15 each include "wherein the barrier layer comprises an etch characteristic such that the barrier material can be selectively etched in the presence of the seed material." [Emphasis added] It is axiomatic that for these claims to be anticipated Obeng must describe these limitations in addition to those of the base claims. To address these limitations, the Patent Office states on page 3 of the Final Office Action, "Obeng et al. teaches an integrated an integrated circuit, wherein the barrier material and seed material comprise different materials that would have inherently used different etch chemistries/rates." [Emphasis added] In order for a limitation to be inherent, it must necessarily flow from the teachings of the prior art. Thus, the fact that a feature may occur in a reference is not sufficient to establish its inherency. For example, although the barrier material and seed material in Obeng may be different materials, it does not necessarily flow that those materials have different etch chemistries or rates, because according to the damascene process used in Obeng (Obeng, col. 3, line 64), the barrier layer is a refractory material which inhibits the diffusion of the interconnect material into the dielectric, and the seed material lines the barrier material so that the interconnect material will form properly within the via and trench. However, although the barrier material and seed material are different materials, they may have the same etch rate, similar etch rates such that the barrier material cannot be selectively etched in the presence of the seed material. In addition, the seed material may be more susceptible to etching than the barrier material such that the barrier material cannot be selectively etched in the presence of the seed material. Therefore, it does not necessarily flow that the barrier material and seed material of Obeng use different etch chemistries/rates. Moreover, in the Advisory Action mailed

November 13, 2002, the Patent Office states "additionally, other processes can be employed to etch the barrier material in the presence of the seed material." However, the position cited does not describe a barrier layer comprising an etch characteristic such that the barrier material can be selectively etched in the presence of the seed material, as required by dependent claim 16. Furthermore, the Applicant traverses this statement in accordance with MPEP §2144.03, and requests that the Patent Office provide a reference in support of this position. Hence, for these additional reasons, the Applicant respectfully submits that the Board should overturn the rejection of dependent claim 15 under 35 U.S.C. §102(e) as being anticipated by Obeng.

5) **Specific limitation of Group III not described in the cited references.**

Independent claim 16 requires a conductive material in the via; wherein the seed layer and barrier material are formed so as to expose the circuit device at an end of the via.

6) **Explanation as to why such limitations render Group III unanticipated by the cited references.**

Applicant submits that independent claim 16 is not anticipated by Obeng for at least the reason that Obeng does not describe a conductive material in a via having a seed layer and a barrier material formed so as to expose a circuit device at an end of the via. It is axiomatic that to be anticipated, every element of claim 16 must also be disclosed within Obeng. In the Patent Office's rejection of independent claim 16, the Patent Office cites the same portions of Obeng cited against independent claim 12, above.

However, as described above, for a conductive material directly contacting the surface of a circuit device as claimed in claim 12, the Patent Office has not identified and the Applicant is unable to find any description in Obeng of a conductive material in a via having a seed layer and barrier material formed to expose the circuit device at an end of the via. Therefore, these limitations of claim 16 are distinct from the known techniques of capping a barrier film and copper seed layer of Obeng. Hence, the Applicant respectfully submits that the Board should overturn the rejection of independent claim 16 under 35 U.S.C. §102(e) as being anticipated by Obeng.

7) **Specific limitations of Group IV not described in the cited references.**

Throughout the following argument, it is assumed that the dependent claims carry with them the arguments made in favor of base claims and any intervening claims.

Claim 17 further requires that the barrier layer comprises an etch characteristic such that the barrier material can be selectively etched in the presence of the seed material.

8) **Explanation as to why such limitations render Group IV unanticipated by the cited references.**

Applicant submits that dependent claim 17 is further not anticipated by Obeng for at least the reason that Obeng does not describe a barrier layer with etch characteristics so that the barrier material can be selectively etched in the presence of the seed material.

Applicant's dependent claim 17 includes "wherein the barrier layer comprises an etch characteristic such that the barrier material can be selectively etched in the presence of the seed material." It is axiomatic that for these claims to be anticipated Obeng must describe these limitations in addition to those of the base claims. To address this limitation, the Patent Office states on page 3 of the Final Office Action, the same rejection cited above with respect to dependent claim 15. However, as stated above with respect to dependent claim 15, it does not necessarily flow that the barrier material and seed material have different etch chemistries or rates simply because they are different materials, as it is possible that they have the same etch rate, similar etch rates, or that the seed material be more susceptible to etching than the barrier material, such that the barrier material cannot be selectively etched in the presence of the seed material. In addition, as mentioned above with respect to dependent claim 15, the Patent Office's assertion in the Advisory Action does not cure the lack of description in Obeng of the above-cited claim limitations, and is traversed by the Applicant in accordance with MPEP §2144.03. Hence, for these additional reasons, the Applicant respectfully submits that the Board should overturn the rejection of dependent claim 17 under 35 U.S.C. §102(e) as being anticipated by Obeng.

IX. CONCLUSION AND RELIEF

Based on the foregoing, Applicant requests that the Board overturn the Examiner's rejection of all pending claims and hold that all of the claims of the present application are allowable.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Dated: January 24, 2003.

Angelo J. Gaz, Reg. No. 45,907

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on January 24, 2003.

Margaux Rodriguez *January 24. 2003*

X. APPENDIX A

The claims involved in this Appeal are as follows:

12. An integrated circuit comprising:

a substrate having a circuit device;

a dielectric material overlying the circuit device with a via formed in the dielectric material to the circuit device, the via exposing a sidewall in the dielectric material and a surface of the circuit device;

a barrier material substantially lining the sidewall;

a seed layer on the barrier material and substantially lining the sidewall; and

a conductive material directly contacting the surface of the circuit device.

13. The integrated circuit of claim 12, wherein the circuit device comprises an interconnection line.

14. The integrated circuit of claim 12, wherein the conductive material is copper.

15. The integrated circuit of claim 12, wherein the barrier layer comprises an etch characteristic such that the barrier material can be selectively etched in the presence of the seed material.

16. An integrated circuit comprising:

a substrate having a circuit device;

a dielectric material overlying the circuit device with a via formed in the dielectric material to the circuit device, the via exposing a sidewall in the dielectric material and a surface of the circuit device;

a barrier material substantially lining the sidewall;

a seed layer on the barrier material and substantially lining the sidewall; and

a conductive material in the via;

wherein the seed layer and barrier material are formed so as to expose the circuit device at an end of the via.

17. The integrated circuit of claim 16, wherein the barrier layer comprises an etch characteristic such that the barrier material can be selectively etched in the presence of the seed material.